Abstract of the Disclosure

The present invention provides a method for fabricating a semiconductor device capable of decreasing a parasitic capacitance to thereby increase a cell capacitance. To achieve this effect, the deposited third inter-layer insulation layer is planarized and is subjected to a wet etching process to make its height lower than that of the bit line. Afterwards, the nitride-based etch stop layer is formed on the etched third inter-layer insulation layer, and then, the contact hole for forming the storage node contact plug is formed in between the bit lines through the SAC process so that the etch stop layer does not remain at sidewalls of the bit line. From this structure, it is possible to decrease the parasitic capacitance, and this decrease further provides an effect of increasing the cell capacitance.